ABSTRACT OF THE DISCLOSURE

A driving circuit of a display device such as a liquid crystal generates power supply clocks (1 and 2) based on a system clock during the normal display operation which is not a power save mode. The generated power supply clocks are supplied, directly or after inversion, to the switches (SW1 through SW4 (and SW5 through SW8)) in a charge pump type power supply circuit (300) for switching the connection of capacitors (C1 and C2 (and C11 and C12)) in the power supply circuit (300). In this manner, supply voltages VDD2 and VDD3 which function as the driving power supply for a driving circuit (100) and a display panel (200) can be obtained at the power supply circuit (300) by boosting the input voltage Vin. The driving circuit (100) stops supply of the power supply clocks to the power supply circuit (300) when a transition to the power save mode is instructed and a power save control signal generated by a CPU I/F circuit (16) is changed, thereby suspending generation of the supply voltage an consumption of power consumption at the circuit and display panel.